Amendments to the Specification

Kindly amend paragraph 0039 as follows:

A core 412 is shown coupled to a status register 420, and a PEVG 416, as in ~~Figure 3.~~ Figure 4. The core 412 executes instructions retrieved from a memory (not shown) including interrupt handler routines referenced by a memory vector 418 provided by the PEVG 416. In addition, as will be further described below, the core 412 reads and writes values from/to particular registers within the status register 420, including a vector table 422, an interrupt register 424 (having a number of interrupt specific registers 426), and interrupt priority registers 428. In one embodiment, the core 412 only writes to these registers when executing operating system or kernel mode instructions. Although not specifically labeled, in one embodiment the status register 420 contains an interrupt register 424 that has a 12-bit field, where each bit field 426 corresponds to one of twelve possible interrupts that may be handled by the processor 400. The bit fields 426 may be used as an interrupt mask for each of the interrupts 0-11 (e.g., a value of "1" in a bit field would indicate that the interrupt is enabled, a value of "0" would indicate that the interrupt is not enabled). One skilled in the art will appreciate that if more interrupts are desired to be handled by the processor 400, additional bit fields 426 may be added to the register 424.